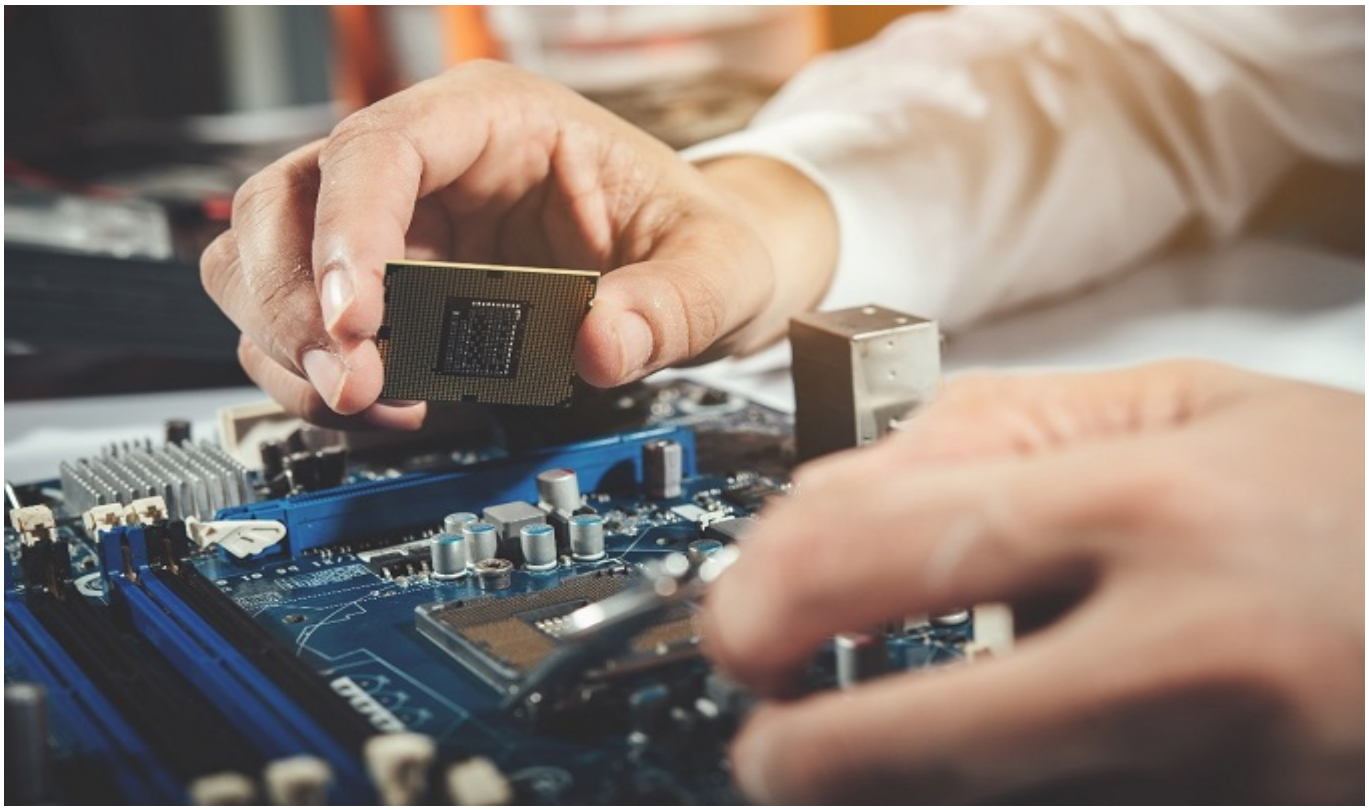
National Occupational Standards



VLSI Design Fundamentals

Unit Code: ELE/N1419

Version: 1.0

NSQF Level: 4

Electronics Sector Skills Council of India || 155, 2nd Floor, ESC House Okhla Industrial Area-Phase 3
New Delhi- 110020 || email:ceo@essc-india.org

Description

Explore the basic theory and practice of VLSI design by covering transistor-level circuit design to chip assembly, gain hands-on experience and deep understanding of VLSI fundamentals. Develop skills essential for success in designing and verifying complex integrated circuits.

Scope

The scope covers the following :

- The scope covers the following:
- 1) Advanced study in VLSI design fundamentals
- 2) Practical application of transistor-level analysis and optimization
- 3) Exploration of circuit performance and optimization techniques
- 4) Hands-on experience in advanced design topics and verification methods
- 5) Preparation for roles in semiconductor industry

Elements and Performance Criteria

Transistor Fundamentals and CMOS Basics

To be competent, the user/individual on the job must be able to:

PC1. Understand the fundamental properties of nMOS and pMOS transistors for digital switching

PC2. Illustrate basic logic gate configurations using nMOS and pMOS transistors through schematic diagrams.

PC3. Analyze the cross-sectional structure of a CMOS inverter and list its fabrication steps.

PC4. Explore the operation of CMOS latches and flip-flops.

PC5. Familiarize with stick diagrams for efficient layout planning in CMOS circuit design.

Advanced Circuit Design Techniques

To be competent, the user/individual on the job must be able to:

PC6. Generate transistor-level schematics and layouts for complementary CMOS standard cells emphasizing optimization.

PC7. Analyze the operation of D latch and D flip-flop using time diagrams.

PC8. Explore techniques for managing the design of complex systems.

PC9. Dive into abstraction levels of processor implementation covering architecture, microarchitecture, logic design, and physical design

PC10. Synthesize logic gates from hardware description language and perform place and route operations using appropriate tools.

Transistor-Level Analysis and Optimization

To be competent, the user/individual on the job must be able to:

PC11. Investigate MOS transistor behavior across different regions using cross-sectional diagrams.

PC12. Derive and interpret I-V curves of MOS devices, focusing on gate and diffusion capacitance.

PC13. Analyze nonideal transistor behaviors induced by high field effects and threshold voltage variations.

PC14. Apply mathematical models to estimate MOS gate capacitance and understand its effects on circuit performance.

PC15. Utilize SPICE simulation to analyze circuit performance and optimize designs.

Circuit Performance and Optimization

To be competent, the user/individual on the job must be able to:

PC16. Explain threshold drop in pass transistor circuits and analyze DC response of CMOS logic gates.

PC17. Utilize RC delay models to estimate gate delays and optimize performance.

PC18. Apply Logical Effort techniques to optimize combinational circuit paths and manage power consumption.

PC19. Explore the implications of technology scaling on transistor characteristics and power dissipation.

PC20. • Simulate circuit behavior using Simulation Program with Integrated Circuit Emphasis (SPICE) to analyze DC transfer characteristics, transient
• response, and power consumption.

Advanced Design Topics

To be competent, the user/individual on the job must be able to:

PC21. Architect and analyze datapath circuits including comparators, shifters, and multi-input adders.

PC22. Compare various adder architectures such as Carry-Ripple, Carry-Lookahead, and Tree Adders.

PC23. Describe clock distribution networks and their impact on skew and power consumption, including DLL and phase-locked loops (PLL).

PC24. Understand the operations of 6T, 12T SRAM using transistor level or gate level diagrams.

PC25. Explore high-speed I/O transceivers and clock recovery techniques.

Verification, Testing, and Packaging

To be competent, the user/individual on the job must be able to:

PC26. Create comprehensive test vectors to detect stuck-at faults in digital circuits, ensuring thorough testing coverage.

PC27. Implement scan chains to enhance observability and controllability during testing, facilitating efficient fault detection and debugging.

PC28. Design and integrate built-in self-test (BIST) circuits within the chip to automate the testing process and enhance reliability.

PC29. Apply IEEE standard boundary scan methodology for structural testing of integrated circuits, ensuring adherence to industry standards.

PC30. • Understand the functionality of Electrostatic Discharge (ESD) protection circuits to safeguard chips against electrostatic damage, enhancing
• overall chip reliability.

Knowledge and Understanding (KU)

The individual on the job needs to know and understand:

KU1. Understand the principles of nMOS and pMOS transistors.

KU2. Grasp the operation of basic logic gates.

KU3. Comprehend the fabrication steps of CMOS inverters.

KU4. Design complementary CMOS standard cells.
KU5. Interpret time diagrams for sequential circuits.
KU6. Apply design techniques for complex systems.
KU7. Implement processor architecture at various abstraction levels.
KU8. Analyze MOS transistor characteristics in different regions.
KU9. Estimate transistor parameters for circuit optimization.
KU10. Understand clock distribution networks and their impact.
KU11. Describe sources and effects of on-chip variation and noise.

Generic Skills (GS)

User/individual on the job needs to know how to:

GS1. Technical Proficiency
GS2. Analytical thinking
GS3. Problem-solving
GS4. Attention to detail
GS5. Critical thinking
GS6. Time management
GS7. Collaboration
GS8. Data interpretation
GS9. Attention to performance metrics
GS10. Problem-solving
GS11. Adaptability

Assessment Criteria

Assessment Criteria for Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
Transistor Fundamentals and CMOS Basics	**5**	**5**	**-**	**-**
PC1. Understand the fundamental properties of nMOS and pMOS transistors for digital switching	1	1	-	-
PC2. Illustrate basic logic gate configurations using nMOS and pMOS transistors through schematic diagrams.	1	1	-	-
PC3. Analyze the cross-sectional structure of a CMOS inverter and list its fabrication steps.	1	1	-	-
PC4. Explore the operation of CMOS latches and flip-flops.	1	1	-	-
PC5. Familiarize with stick diagrams for efficient layout planning in CMOS circuit design.	1	1	-	-
Advanced Circuit Design Techniques	**10**	**10**	**-**	**-**
PC6. Generate transistor-level schematics and layouts for complementary CMOS standard cells emphasizing optimization.	2	2	-	-
PC7. Analyze the operation of D latch and D flip-flop using time diagrams.	2	2	-	-
PC8. Explore techniques for managing the design of complex systems.	2	2	-	-
PC9. Dive into abstraction levels of processor implementation covering architecture, microarchitecture, logic design, and physical design	2	2	-	-
PC10. Synthesize logic gates from hardware description language and perform place and route operations using appropriate tools.	2	2	-	-
Transistor-Level Analysis and Optimization	**10**	**10**	**-**	**-**
PC11. Investigate MOS transistor behavior across different regions using cross-sectional diagrams.	2	2	-	-

Assessment Criteria for Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
PC12. Derive and interpret I-V curves of MOS devices, focusing on gate and diffusion capacitance.	2	2	-	-
PC13. Analyze nonideal transistor behaviors induced by high field effects and threshold voltage variations.	2	2	-	-
PC14. Apply mathematical models to estimate MOS gate capacitance and understand its effects on circuit performance.	2	2	-	-
PC15. Utilize SPICE simulation to analyze circuit performance and optimize designs.	2	2	-	-
Circuit Performance and Optimization	**10**	**5**	**-**	**-**
PC16. Explain threshold drop in pass transistor circuits and analyze DC response of CMOS logic gates.	2	1	-	-
PC17. Utilize RC delay models to estimate gate delays and optimize performance.	2	1	-	-
PC18. Apply Logical Effort techniques to optimize combinational circuit paths and manage power consumption.	2	1	-	-
PC19. Explore the implications of technology scaling on transistor characteristics and power dissipation.	2	1	-	-
PC20. • Simulate circuit behavior using Simulation Program with Integrated Circuit Emphasis (SPICE) to analyze DC transfer characteristics, transient • response, and power consumption.	2	1	-	-
Advanced Design Topics	**10**	**5**	**-**	**-**
PC21. Architect and analyze datapath circuits including comparators, shifters, and multi-input adders.	2	1	-	-
PC22. Compare various adder architectures such as Carry-Ripple, Carry-Lookahead, and Tree Adders.	2	1	-	-

Assessment Criteria for Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
PC23. Describe clock distribution networks and their impact on skew and power consumption, including DLL and phase-locked loops (PLL).	2	1	-	-
PC24. Understand the operations of 6T, 12T SRAM using transistor level or gate level diagrams.	2	1	-	-
PC25. Explore high-speed I/O transceivers and clock recovery techniques.	2	1	-	-
Verification, Testing, and Packaging	**10**	**10**	**-**	**-**
PC26. Create comprehensive test vectors to detect stuck-at faults in digital circuits, ensuring thorough testing coverage.	2	2	-	-
PC27. Implement scan chains to enhance observability and controllability during testing, facilitating efficient fault detection and debugging.	2	2	-	-
PC28. Design and integrate built-in self-test (BIST) circuits within the chip to automate the testing process and enhance reliability.	2	2	-	-
PC29. Apply IEEE standard boundary scan methodology for structural testing of integrated circuits, ensuring adherence to industry standards.	2	2	-	-
PC30. • Understand the functionality of Electrostatic Discharge (ESD) protection circuits to safeguard chips against electrostatic damage, enhancing • overall chip reliability.	2	2	-	-
NOS Total	**55**	**45**	**-**	**-**

National Occupational Standards (NOS) Parameters

NOS Code	ELE/N1419
NOS Name	VLSI Design Fundamentals
Sector	Electronics
Sub-Sector	
Occupation	Product Design-S&C
NSQF Level	4
Credits	2
Minimum Educational Qualification & Experience	Pursuing 2nd year of 3-year regular Diploma (after 10th) with NA of experience OR 12th Class (Equivalent) with NA of experience OR 10th Class with 3 Years of experience OR Previous relevant Qualification of NSQF Level (Level 3) with 3 Years of experience
Version	1.0
Last Reviewed Date	27/08/2024
Next Review Date	27/08/2027
NSQC Clearance Date	27/08/2024
Reference code on NQR	NG-04-EH-02980-2024-V1-ESSC
NQR Version	1.0
CCN Category	1